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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

	Application No.	Applicant(s)
Office Action Summary	09/484,516	HALEPETE ET AL.
	Examiner	Art Unit	
	Paul R. Myers	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _07 July 2003_ .

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-3,6 and 8-92_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-3,6 and 8-92_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____ .

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
         application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)   4)☐ Interview Summary (PTO-413) Paper No(s). _____ .

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)   5)☐ Notice of Informal Patent Application (PTO-152)

3)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _16,17,19_ .   6)☐ Other: .

Response to Arguments

1.   Applicant's arguments filed 7/7/03 have been fully considered but they are not

persuasive.

In regards to applicants argument that Horden does not teach the newly added limitation

of monitoring conditions internal to a computer processor Claims 12 and 48: The examiner

notes Horden teaches column 5 lines 34-35 that the operating system monitors an application

mix executing in the processor to determine a required frequency and voltages. Figure 1 clearly

shows the conditions variables 15 coming from internal to the processor. Column 4 lines 39-41

teach that other conditions are monitored such as temperature, device behavior, and performance

data. Temperature and performance data are clearly conditions internal to the processor.

In regards to applicants argument that Horden teaches away from using conditions

internal to the computer processor for determining frequency and voltage as claimed in that

Horden teaches that the maximum power consumption is established by user, operating system,

or some sort of external considerations: First the examiner notes that Horden expressly teaches

monitoring and using internal conditions to the processor. Second the user selects the maximum

power consumption not the voltage and frequency. The power consumption is a function of the

voltage, frequency, current, and time at voltage. Third this is "yet another embodiment". And

fourth the user selects the limit not the values returned of what is monitored.

In regards to applicants that Horden teaches an embodiment with only two voltages and

frequencies (Column 3 lines 48-53) in which the operating system notifies the state machine

whether the core should be operating at peak or idle frequencies and voltages. That is, the

decision as to what voltage and frequency at which to operate is made by the operating system

based on considerations external to the processor. First the section cited by the applicant

expressly teaches the core utilization is one of the conditions monitored to determine the two

voltages and two frequencies to use. The core utilization is an internal condition. Second the

this is not the only embodiment and Horden expressly teaches internal conditions such as

temperature and performance data. The examiner agrees that Horden teaches monitoring both

internal and external conditions for determining the operating voltages and frequencies. The

claim language state monitoring conditions internal to the processor for determining the

frequencies and voltages to operate. The claim language does not state that external conditions

cannot also be monitored.

In regards to applicants argument that claim 20 recites monitoring idle time of a computer

processor: Horden teaches monitoring the core utilization. Core utilization includes idle time.

Horden also states the time spend at each frequency is a consideration in power saving (Column

5 lines 3-6).

In regards to applicants argument that claim 29 recites monitoring the state of the

computer processor: Horden teaches the monitoring the idle state, and the application mix

executing in the processor which is the state of the processor. The examiner also notes Horden

monitors the temperature which is the state of the processor.

In regards to applicants argument that claims 40, 46 and 67 recites monitoring operating

temperature: Horden expressly teaches monitoring temperature.

In regards to applicants argument regarding the 103 rejection of claim 1: Since the

applicants have amended claim 1 to remove the feature for which the Weiss reference was

applied to claim 1, the Weiss reference will not be applied to claim 1.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

3.   Claims 1, 65, 68, 83, and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Horden et al PN 5,812,860.

In regards to claims 1 and 88: Horden et al teaches a method for controlling the

operating condition of a computer processor comprising the steps of: determining a maximum

allowable power consumption level from the operating condition of the processor (Column 6

lines 23-25); determining the maximum frequency which provides power not greater than the

allowable power consumption level (Column 6 lines 26-30); determining a minimum voltage

which allows operation at the maximum frequency determined (Column 6 lines 33-35); and

dynamically changing the operating condition of the processor by changing the frequency and

voltage to the maximum frequency and minimum voltage determined (Column 6 lines 36-40).

Horden et al also teaches the Clock generator, State machine, and Voltage regulator being on a

single chip. Horden et al does not expressly teach them being on the same chip as the processor.

MPEP 1244.04 V B states making integral is not a patentably distinct. It would have been

obvious to a person of ordinary skill in the art to integrate the stare machine/frequency generator

in the processor because this would have saved space.

In regards to claims 65 and 68: Horden et al teaches calculating the voltage and

frequency pairs. Official notice is taken that lookup tables are well known. It would have been

obvious to a person of ordinary skill in the art at the time of the invention to maintain the voltage

frequency pairs in a lookup table because this would have saved the time in calculating the

voltage frequency pairs.

In regards to claims 83: Horden teaches the operating system controlling the voltage and

frequencies therefore Horden teaches executing instructions in said computer processor before,

during and after changing voltage and frequency.

4.   Claims 2-3, 6, 8-11, 78-79 and 87 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Horden et al PN 5,812,860 in view of Weiss et al PN 5,774,703.

In regards to claims 2, 6, 8, 78-79 and 87: Horden et al teaches a power supply

furnishing selectable output voltages (7 and 5); a clock frequency source (8 and 6); a central

processor (Figure 1) including: a processing unit (1, 4) for providing values (15) indicative of

operating conditions of the central processor; and a clock frequency generator (6) receiving a

clock frequency (14) from a clock frequency source (8) and providing a selectable output clock

frequency (11) to the processing unit (1, 4); and means for detecting the value indicative of

operating conditions of the central processor (6 via 5 and 4) and causing the power supply (7, 5

via 12) and clock frequency generator (6) to furnish an output clock frequency (11) and voltage

level (9) for the central processor. Horden et al does not teach the clock generator being able to

provide a plurality of frequencies that can be individually selected concurrently. Weiss et al

teaches a clock generator for a processor that provides a plurality of clock frequencies which can

be individually selected concurrently. It would have been obvious to provide multiple

concurrent frequencies because this would have made it easier to optimize different subsystems

of the processor (See Weiss abstract). The examiner notes Weiss et al also has the bonus of

teaching the clock generator being integrated on the same chip as the rest of the processor (See

column 2 where it states figure 1 is a single chip processor).

In regards to claims 3 and 9: Horden et al teaches the means for detecting the values

including software (4) for determining the output frequency and power.

In regards to claims 10-11: Horden et al teaches adjusting the operating condition of the

processor core for optimum operation. Horden et al does not expressly teach the core including a

plurality of functional units. Official notice is taken that processor cores with a plurality of

functional units is very well known in the art. It would have been obvious to a person of

ordinary skill in the art at the time of the invention to include a plurality of functional units in the

core because this would have allowed for greater processing capabilities.

5.   Claims 13-15, 17-19, 21-23, 26-28, 33-35, 38, 42, 44, 49-51, 53-55, 69-71, 73-75, 80-82,

and 84-86 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horden et al PN

5,812,860 in view of Michail et al PN 5,832,284.

In regards to claims 13-15, 21-23, 33-35, 42, 44, 49-51, 69-71, 80-82: Horden et al

teaches transitioning to higher frequencies and voltages and transitioning to lower frequencies

and voltages. Horden et al however does not teach the claimed order of changing clock and

voltage. Michail et al teaches when increasing frequency increasing voltage then increasing

frequency, and when decreasing frequency decreasing frequency then decreasing voltage (Figure

2). The examiner also notes Michail et al also teaches over-clocking. Michail et al teaches that

the reason for the order is stability of the system. It would have been obvious to change the

voltages and frequencies in the system in the order of Michail because this would have increased

system stability.

In regards to claims 17-19, 26-28, 38, 53-55, 73-75, 84-86: Horden et al teaches

executing instructions before, during and after changing voltage and frequency.

6.   Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horden et al PN

5,812,860 in view of Klein PN 5,913,067.

In regards to claim 24: Horden teaches monitoring device utilization which includes data

and idle time. Horden also teaches monitoring internal performance data, however Horden et al

does not expressly teach that the monitoring of the idle time comprises the monitoring of the

internal data. Klein teaches monitoring data transfer to determine device activity to determine

device idle time (Column 2 lines 11-23). It would have been obvious to use internal data

transfers to determine idle time because this is a standard method of determining idle time

especially in consideration of utilization.

7.   Claims 30-32, 57-59, and 62-64 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Horden et al PN 5,812,860 in view of Fung et al PN 5,710,929

In regards to claim 30-32, 57-59, 62-64: Horden teaches monitoring processor activity.

Horden et al does not teach the activity including a sleep state or a halt state. Fung teaches an

activity monitor that handles multiple sleep states including a halt instruction that halts the

processor. It would have been obvious to a person of ordinary skill in the art to include multiple

sleep states such as Sleep, Doze, and Halt because this would have allowed for multiple user

selectable power levels.

8.   Claims 41 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horden

et al PN 5,812,860 in view of Cepuran PN 5,628,001

In regards to claim 41 and 47: Horden et al teaches operating above a frequency and a

voltage. Horden however does not expressly teach determining a time period which the system

may operate at the higher voltage and frequency. Cepuran teaches increasing the clock

frequency for transmission of data, transmitting the data and if a time period (The examiner notes

Cepuran misspells period "perion") elapses reducing the frequency. It would have been obvious

to a person of ordinary skill in the art at the time of the invention to include a time period for the

high frequency because this would have provided for power savings as well as prevented

thrashing.

9.   Claims 91 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michail et al

PN 5,832,284 in view of Cepuran PN 5,628,001.

In regards to claim 91: Michail et al teaches operating above a frequency and a voltage.

Michail however does not expressly teach determining a time period which the system may

operate at the higher voltage and frequency. Cepuran teaches increasing the clock frequency for

transmission of data, transmitting the data and if a time period (The examiner notes Cepuran

misspells period "perion") elapses reducing the frequency. It would have been obvious to a

person of ordinary skill in the art at the time of the invention to include a time period for the high

frequency because this would have provided for power savings as well as prevented thrashing.

Claim Rejections - 35 USC § 102

10.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11.   Claims 12, 16, 20, 25, 29, 36-37, 39-40, 43, 45-46, 48, 56, 60-61, 66-67, 72, 72 and 76-

77 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Horden et al PN

5,812,860.

In regards to claims 12, 48 and 76: Horden et al teaches monitoring operating conditions

internal to a computer processor; determining a frequency and a voltage at which to operate said

computer processor, based on said internal operating conditions; and implementing the

determined frequency and voltage.

In regards to claims 16, 25, 36-37, 39, 52, 72: Horden teaches the operating system

controlling the voltage and frequencies therefore Horden teaches executing instructions in said

computer processor before, during and after changing voltage and frequency.

In regards to claim 20: Horden et al teaches monitoring operating conditions including

core utilization which includes idle time; determining a frequency and a voltage at which to

operate said computer processor, based on said internal operating conditions; and implementing

the determined frequency and voltage.

In regards to claims 29, 56 and 61: Horden et al teaches monitoring the state of the processor; determining a frequency and a voltage at which to operate said computer processor, based on said internal operating conditions; and implementing the determined frequency and voltage.

In regards to claims 40, 43, 46, 60 and 67: Horden et al teaches monitoring the temperature of the processor; determining a frequency and a voltage at which to operate said computer processor, based on said internal operating conditions; and implementing the determined frequency and voltage.

In regards to claim 45: Horden executes instructions. These inherently include processor intensive commands.

In regards to claim 66: Horden et al teaches calculating the voltage frequency pairs.

In regards to claim 77: Horden et al teaches a plurality of selectable frequencies.

12.   Claims 89-90 and 92 are rejected under 35 U.S.C. 102(b) as being anticipated by Michail et al PN 5,832,284.

In regards to claim 89: Michail et al teaches operating a computer with an operating temperature below a pre-selected temperature (T<Topt) with an input voltage at a safe voltage level (NV column 3 lines 58-60) and an input frequency at a safe frequency (NC Column 3 lines 64-66); increasing said input voltage to a level higher than said safe voltage level (Figure 2 step 3 AV); increasing said input frequency to a level higher than said safe frequency (Figure 2 step 4 AC); executing processor-intensive commands (Full utilization) while said input voltage is at a

level higher than said safe voltage and said frequency is at a level higher than said safe frequency

(When system in state 4).

In regards to claim 90: Michail et al teaches continuing execution of processor intensive

commands until said operating temperature exceeds a pre-defined value(step 5 Topt < T <

Tswitch enters UC).

In regards to claim 92: Michail et al teaches decreasing voltage and frequency (going

from 4 to 2 or from 5-7.

Conclusion

13.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Paul R. Myers whose telephone number is 703 305 9656. The

examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mark Rinehart can be reached on 703 305 4815. The fax phone number for the

organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is 703 305 3900.

PAUL R. MYERS
PRIMARY EXAMINER

PRM
September 4, 2003